

OVERVIEW

LogicVision’s ETMemory provides a complete solution for at-speed testing, diagnosis and repair of embedded memories. On-chip generated algorithmic test patterns are delivered to the memories at application clock frequencies. The ETMemory controllers are configurable to support a variety of memory types, as well as a range of memory timing interfaces and memory port configurations. These controllers are accessed and controlled through LogicVision’s Test Access Port (TAP) interface hierarchy using IEEE 1149.1 and IEEE 1500 protocols. The controllers can be accessed throughout the life of the integrated circuit, including manufacturing test, silicon debug, and system verification phases. ETMemory includes LogicVision’s unique comprehensive automation suite that provides test rule checking, test planning, integration and verification all at the RTL or gate level. It also includes LogicVision’s LVPD capability, which allows the encapsulation of automatic fail datalog functionality into a dynamically linked library (DLL) that is linked directly into the user test program.

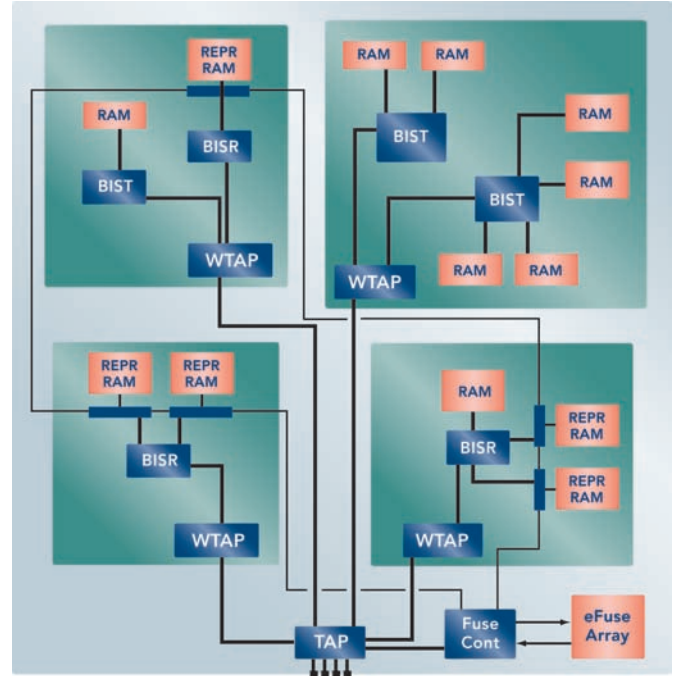


Fig. 1 Hierarchical Architecture

To best address each customer’s specific embedded memory test and repair needs, ETMemory consists of a base solution, offered with several major options representing key memory test and repair capabilities.

OPTION	DESCRIPTION	KEY BENEFITS
Hard Algorithm Programming	Supports design time hardcoding of user test algorithms. Innovative architecture supports the programming of any test algorithm.	Quality and test time optimization through run-time selection of most appropriate test algorithm.
Soft Algorithm Programming	Supports run time programming of user test algorithms. Full automation provided for downloading program code through the TAP.	Full control of quality/test time trade-offs. Provides insurance for unanticipated defect issues.
Repair Analysis Row OR Column	Built-In hardware automatically computes reconfiguration instructions (fuse values) for repairable memories containing defects.	Major test time reduction when dealing with repairable memories, as defect data need not be extracted from the chip.
Repair Analysis Row AND Column	Built-In Repair Analysis for memories containing both Row and Column spares. Computes optimal reconfiguration regardless of fault distribution.	Major test time reduction when dealing with memories with both spare rows and spare columns to achieve maximum yield levels.
Self Repair	Provides full autonomous on-chip memory repair. Supports Row only, Column only, or Row and Column redundant memories.	In-system memory repair for long term reliability. Improves final test yield through test of repaired memories at sort.

Hard and Soft Algorithm Programming

At design time, one or more user specified memory test algorithms can be hard coded into an ETMemory Built-In Self-Test (BIST) controller. Any of these algorithms can then be applied to each memory through run time control. This capability is useful for optimizing test time by selecting shorter test algorithms as the manufacturing process matures. Any ETMemory BIST controller can also be made to be fully run time programmable. With this feature implemented, any user-specified memory test algorithm can be downloaded into the BIST controller while on the tester. This capability allows any unforeseen defect mechanism to be dealt with without a design respin. Both the hard and soft programming features can be used within the same BIST controller. In both cases, the specification of virtually any memory test algorithm is supported.

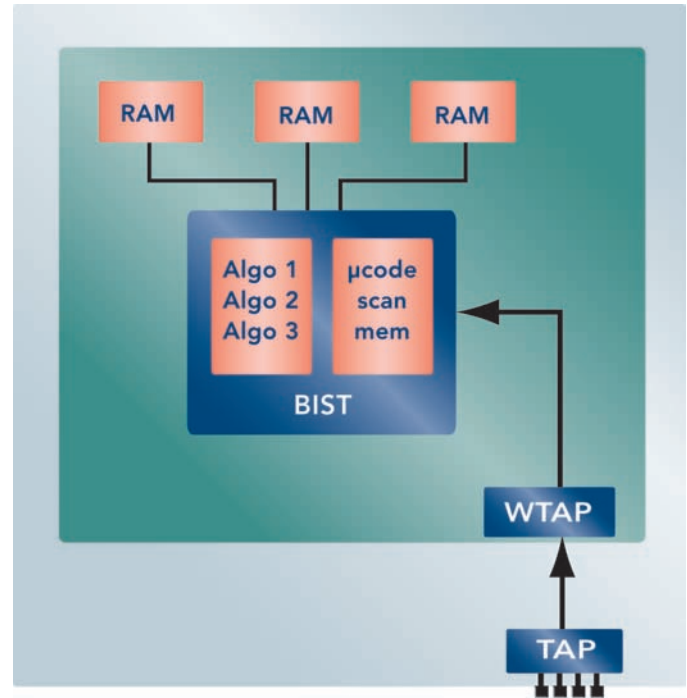


Fig. 2 Combined hard and soft programming

HARD ALGORITHM PROGRAMMING CAPABILITIES:

- Supports the design time hardcoding of user defined test algorithms
- Innovative architecture supports the programming of virtually any memory test algorithm
- High-level programming language for straightforward algorithm specification
- Solution provides a large library of common memory test algorithms
- Complete high-level code is included for direct use or as a reference for user-modified algorithms

SOFT ALGORITHM PROGRAMMING CAPABILITIES:

- Supports all of the features of the hard algorithm programming option
- Also supports the run time (post-silicon) programming of user-defined test algorithms
- Approach uses scannable microcode memory to store program code for algorithm
- Full automation provided for downloading program code through the TAP
- A combination of both hardcoded algorithms and microcode for post-silicon algorithm programming can be incorporated into an ETMemory controller
 - › Allows default run without scan initialization
 - › Allows yield ramp learning, as different diagnostic algorithms can be downloaded as needed
 - › Useful for production/board/system reuse, as default algorithm requires no external initialization data

Comprehensive Self-Repair

LogicVision's embedded memory self-repair solution eliminates the complexities and costs associated with external repair flows. It tests and permanently repairs all defective memories in a chip using virtually no external resources. The chip level architecture implementing the self-repair solution is illustrated in figures 1 and 3. The architecture is hierarchical allowing self-test and self-repair capabilities to be added to individual cores as well as at the top level. Central to this architecture is LogicVision's Fuse Controller. Electrical or programmable fuses are becoming increasingly popular, as they are smaller than laser based fuses, and they can be programmed without the need of any external (laser) equipment. Pooling fuses together results in greatly reduced overhead as fuse data is only stored for the memories needing repair on any given die. Management of the storage and retrieval of fuse data is fully handled on-chip by the Fuse Controller. This controller, along with one or more BISR controllers performs all necessary activities for testing and repairing memories. In this hierarchical architecture, BIST controllers are used for testing memories that do not contain redundancy. When memories with redundancy are used, the BIST controller is upgraded to a Built-In Self-Repair (BISR) controller, to both test the memories, and to also analyze how to repair the faulty ones. This latter capability is typically referred to as Built-In Repair Analysis (BIRA).

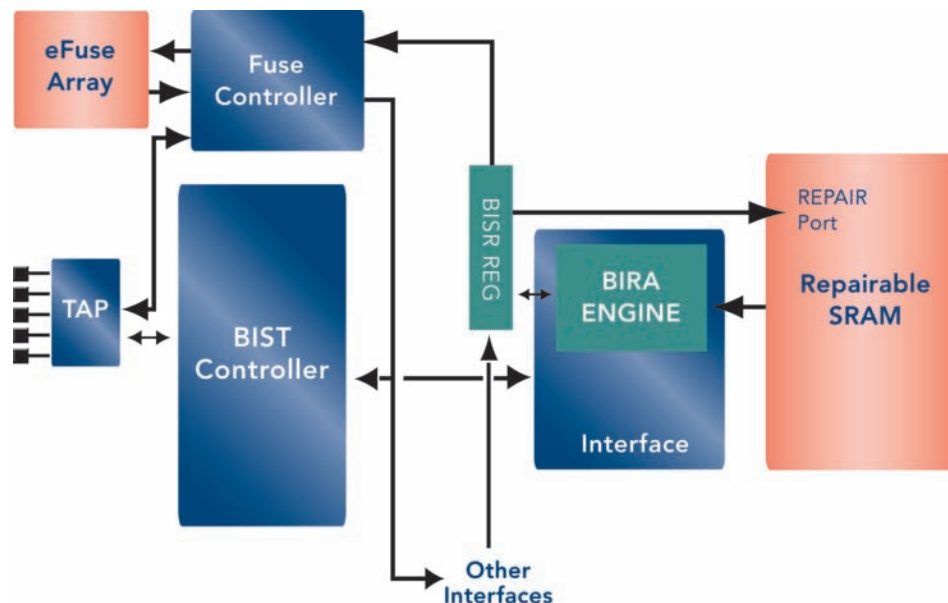


Fig. 3 Self-Repair Architecture Components

CAPABILITIES

- On-chip test and repair of any third party repairable SRAMs
- Optimal repair of memories with row only, column only, or row & column redundancy
- On-chip global eFuse management including fuse data compression and programming as well as fuse data decompression and distribution to memories
- Incremental on-chip memory repair
- Supports any level of parallelism for both test and repair activities

BENEFITS

- Reduced Manufacturing Costs:
 - › Single insertion memory repair on any tester
 - › Multi-site test and repair on any tester
 - › Optimal Row and Column repair analysis for maximum yield
- Shortened Time-to-Market:
 - › Quick self-test and self-repair IP integration
 - › Automated interactive diagnostics
 - › Fully re-usable embedded test inserted cores

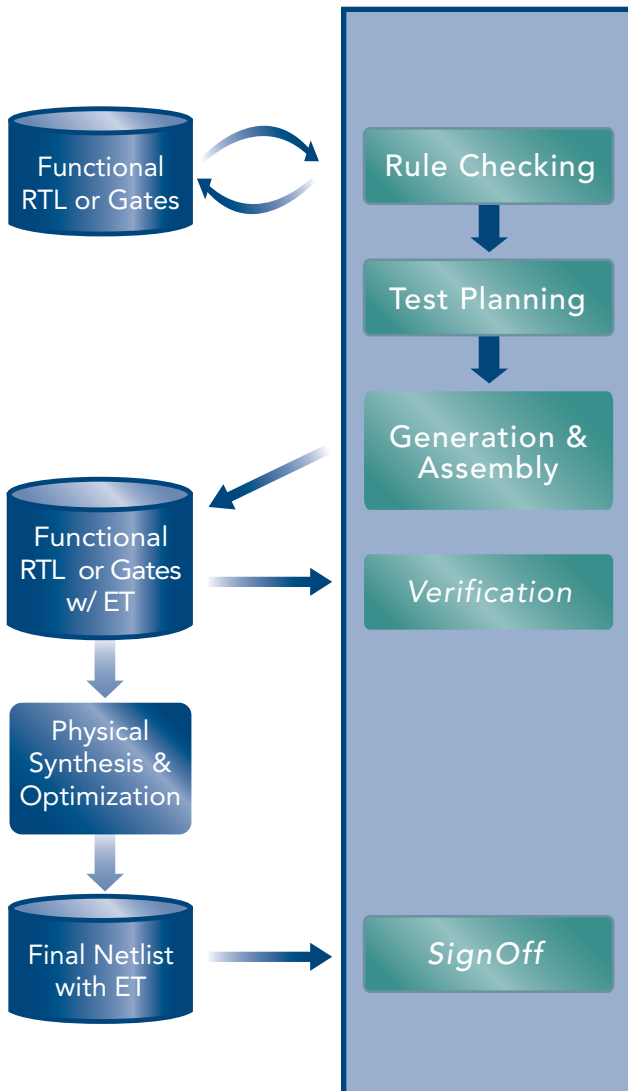


Figure 4. Automated DFT Integration Flow

Automated Integration Flow

All embedded memory test and self-repair capabilities are integrated into the design using LogicVision's advanced automation flow (see figure 4). This hierarchical flow ensures limited impact to the design schedule and quick turn-around time. A key aspect of this flow is its ability to automatically create an optimized embedded memory test and repair infrastructure based on the features of the embedded memories, their distribution throughout the chip and user-provided constraints such as maximum test time and maximum chip power consumption during testing. This unique level of automation is critical as memory counts increase.

All design analysis and embedded test and repair IP generation and integration can be performed at either the RTL or gate levels. The flow is tightly integrated to all major third party physical design flows including RTL-to-GDSII flows.

ABOUT LOGICVISION

LogicVision (NASDAQ: LGVN) provides a comprehensive set of proprietary built-in-self-test (BIST) technologies for achieving the highest quality silicon manufacturing test while reducing test costs for complex System-on-Chip devices. LogicVision's Dragonfly Test Platform™ enables integrated circuit designers to embed BIST functionality into a semiconductor design. This functionality is used during semiconductor production test and throughout the useful life of the chip.

The complete Dragonfly Test Platform, including the ETCreat™, Silicon Insight™ and Yield Insight™ product families, improves profit margins by reducing device field returns and test costs, accelerating silicon bring-up times and shortening both time-to-market and time-to-yield. For more information on the company and its products, please visit the LogicVision website at www.logicvision.com.

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