

FullBIST to FieldBIST - A Design Methodology for Fast Cycle Time to High Volume Production and Profitability

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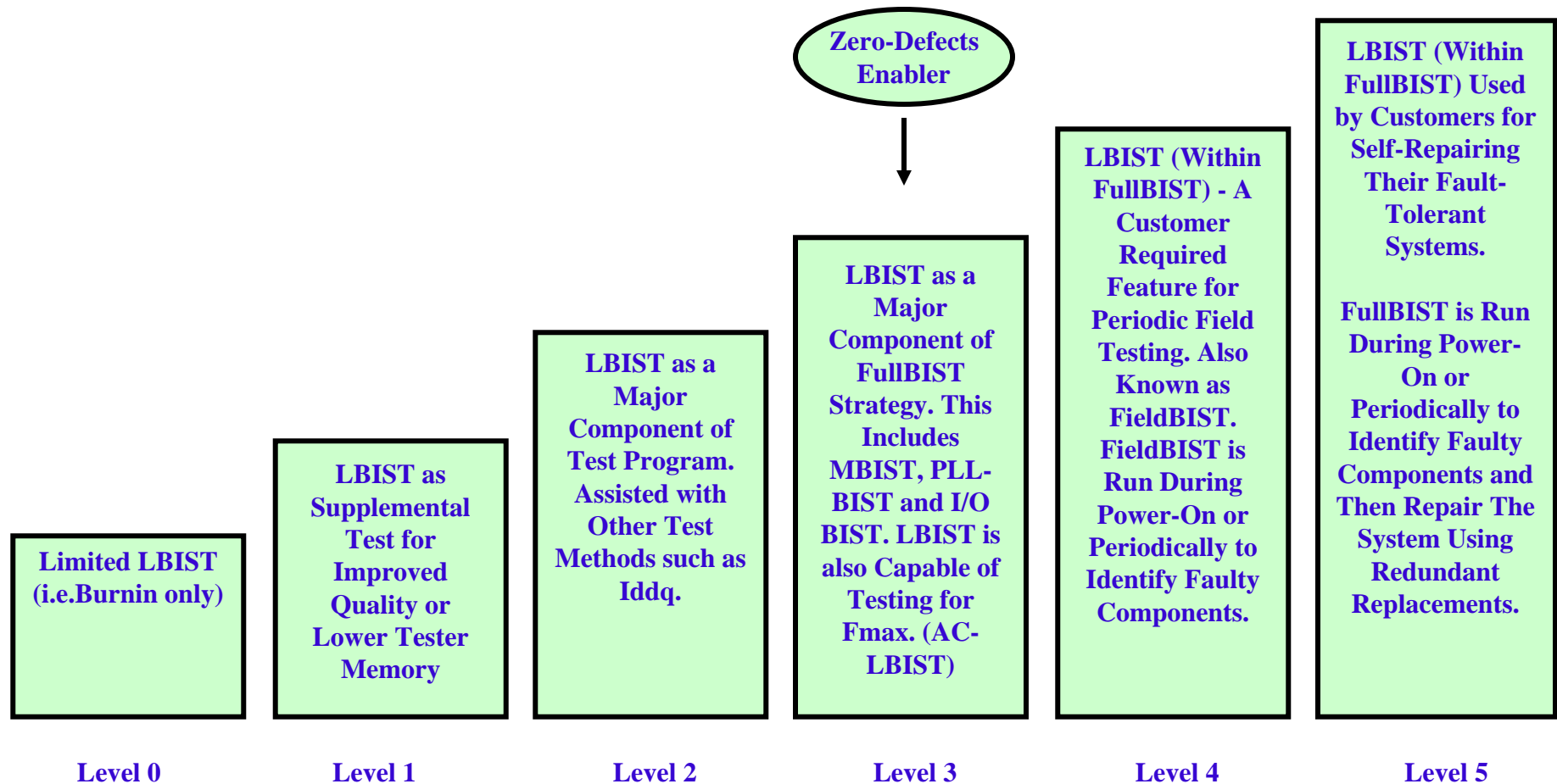
FullBIST to FieldBIST – Outline

- **FullBIST to FieldBIST Objectives**
- **FullBIST versus Traditional Scan**
- **Low Silicon Bring Up and Test Costs**
- **FieldBIST Benefits**
- **Low IC Development Costs versus Benefits**
- **Summary**

FullBIST to FieldBIST – Objectives

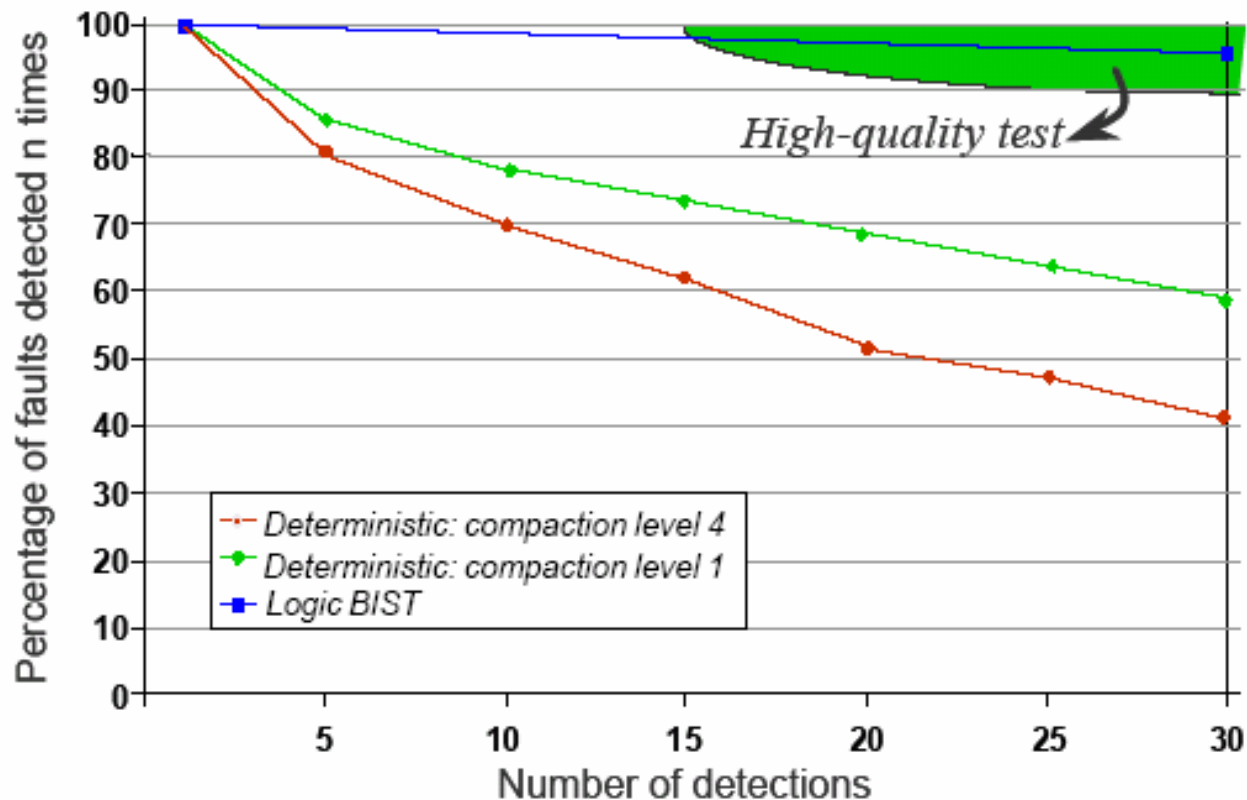
- **Low I.C. Development Cost for Best-In-Class Coverage**
- **Unified I.C. Design and Silicon Validation Environment**
- **Fast Time to Sample, Qualification, Volume Production**
- **Low Test Cost**
- **Check Silicon Health at Customer's Site**

FullBIST Roadmap



- Reference: Raina Rajesh, Freescale Semiconductor DFTMDC, 2004.

N – Detect Coverage



- At comparable coverage levels (Stuck-At or Transition), Logic BIST will have much higher N-detect due to the increased pattern size. This directly impacts Quality of Test.
- Reference: B. Benware, C. Schuermyer, S. Ranganathan, R. Madge, P. Krishnamurthy, N. Tamarapalli, K. Tsai, and J. Rajski, "Impact of Multiple-Detect Test Patterns on Product Quality", Proc. ITC, 2003.

Low Silicon Bring Up Costs

- **Test & FA Engineers Has Full Control**
 - Automated test pattern generation from the same database. Design team is not involvement.
 - Change patterns in <5 minutes versus days via design team.
 - Samples silicon in 3 days versus weeks.
- **Real Time Low Cost Embedded Test Access & Debug Platform**
 - Silicon evaluation & debug using ETA & Validator (LV) via JTAG. All patterns up and running in <1 day versus weeks.
 - PLL characterization in <1 day versus weeks.
 - Locate physical defects using simulation based tool. LV Diagnostic Fault Simulation.
 - Structural and At Speed CZ over PVTs in <1 week versus months.

Low Silicon Test Costs

- **No Functional Patterns (Except for AC Specs)**
 - <20KB versus 8MB with (or 21MB without) ATPG vector compression.
 - Working on removing functional patterns for AC specs in the future.
- **Robust & At Speed Testing @ Probe**
 - x8 (x16 is doable) at probe.
 - **Built In Repair Analysis & Soft Repair**
 - > Reduce probe time & eliminate Sort 2.
 - > Great for further cost reduction using e-Fuse.
 - Reduce assembly costs.
- **Same JTAG Interface & Test Patterns for Burn In.**
- **Significantly Higher Final Test Yield**
 - x4 (x8 is doable) at Final Test.
 - Significantly reduced number of tester power supplies.
 - Small channel requirement.
 - Minimum to no memory requirement for tester.
 - 15% higher final test yield.

FieldBIST – Value Added Results



- **Benefits**
 - Ability to test the device health “on board”.
 - A solution that integrates the controller.
 - Eliminate field returns & associated diagnostic costs.
 - Eliminate costly turn around time.
 - Reduce or eliminate customer’s frustration.
- **High Utilization**
 - Run on first installation to detect board assembly issues.
 - Run periodically to detect stress induced failures.
 - Run on every power up for safety oriented applications.
- **Low Cost**
 - Use standard low cost JTAG interface.
 - Use PC based software.

- **ABIST**
 - Open loop gain – Up and down sides of charge pump.
 - Lock range – Both minimum and maximum.
 - Lock Time – Using either the PLL or ABIST lock detector.
 - Jitter – Short and long (relative, period, self).
- **MBIST**
 - Field modifiable (built in and custom) algorithms.
 - Ability to load new algorithm on the fly during silicon evaluation.
 - BIRA and soft repair to validate fault detection and fuse selection.
 - Automated fuse repair is possible.
- **LBIST**
 - Generate more test patterns than traditional scan.
 - Toggle more logic than functional mode.
 - Stuck at fault detection.
 - At speed transition fault detection – Correlate to functional mode.
 - Single capture (last shift) timing.

Low IC Development Costs vs Benefits

Type	Modules	Source	LV Size (Gates)	% of Die	LV Effort	Traditional Scan Effort
ABIST – 1	PLL	Soft IP -> Generator	4K	0.5%	IP Reuse	NA
LBIST – 3	Core_P, Periph_P, SoC	Generator	33K	3%	1	2 x 6
MBIST – 6	16KB ICache, 192KB M1, 192KB M2, 8KB ROM, 8KB TB, 2 - 2KB Enet, 2KB DMA	Generator	50K	5%	1/2	2 x 6
Control - 2	BSD, Tap Controller	Generator	5K	0.4%	1/2	2 x 1

- **FullBIST Results:**

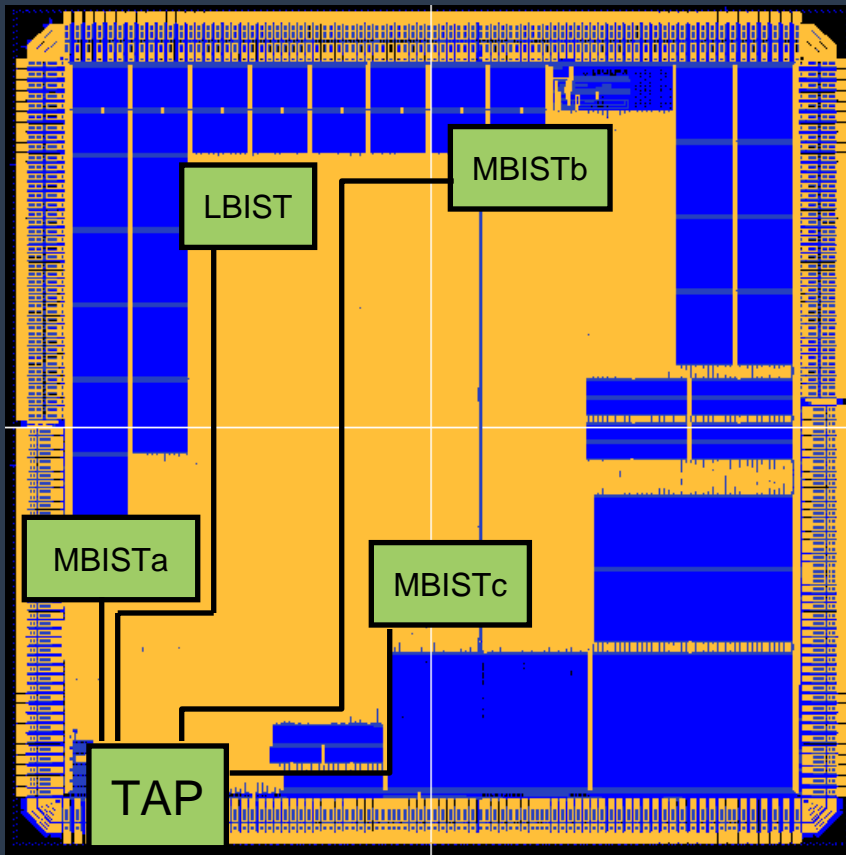
- **MSC7110/2/3/5/6 – 200MHz in 130nm. 97% Stuck-At and 95% Transition Fault Coverage.**
- **MSC7118/9 – 300MHz in 130nm. 98% Stuck-At and 95% Transition Fault Coverage.**

FullBIST to FieldBIST – Met All Objectives

- **Unified I.C. Design and Silicon Validation Environment**
 - LogicVision tool suite, database and Validator.
- **Low I.C. Development Cost with Best-In-Class Coverage**
 - 2 FTEs for full SoC.
 - Negligible speed and minimum size impact (200/300MHz in 130nm).
 - 98% stuck at and 95% at speed fault coverage.
- **Fast Time to Sample, Qualification, Volume Production**
 - All patterns up and running in 1 day.
 - Samples in 3 days.
 - Qualify MSC7110/2/3/5/6 in 9 months and MSC7118/9 in 6 months.
- **Low Total Test Cost**
 - At least 7x reduction in test costs – Compared to functional patterns.
 - Up to 2x reduction in test costs – Compared to ATPG.
 - 15% higher final test yield.
- **Silicon Health Check in Customer Application**
 - Customer identified dead part using FieldBIST in minutes.

MSC7119 - VoIP

Features:



- StarCore™ SC1400S DSP Core
- 300 MHz @ 1.2V in 0.13um
- 256KB M1, 16KB ICache, 8KB Trace Buffer
- 192KB M2, 8KB ROM
- 32 Channel DMA
- 16/32-Bit DDR Interface
- 10/100 Mbps Enet MAC MII/RMII
- 16-Bit Host Interface
- 2 TDMs
- Dual Cascade-able Quad-Timers
- I2C
- UART
- System Controller (WDT, Event Port, BTMs)
- External Interrupts
- GPIO
- PLL / Clock
- OCE™ Debugger / JTAG Interface

